Significant yield improvement for semiconductor production line using NeuMath Yield Optimizer

Paul Fearon[1], Loren Krott[1], Aaron Dries[1]
Jill Card[2], William Martin[2], An Carlson[2], Wai Chan[2]

[1] National Semiconductor Corp, 5 Foden Road
South Portland, Maine 04106
{Paul.Fearon, Loren.Krott, Aaron.Dries}@nsc.com

[2] NeuMath Inc, 22 Bailey's Lane, West Newbury, MA 01985
{jcard,bmartin,acao,wchan}@neumath.com

Abstract. We report significant yield improvement using NeuMath Yield Optimizer on a production line over a 4-month time span at National Semiconductor Portland Maine facility. The Yield Optimizer was installed in mid-May 2005 on the CMOS product line and includes data through mid-September 2005. We detail four of the process modifications made based on the Yield Optimizer recommendations, and conclude that those modifications contribute to significant yield improvements: For wafers that met most of the new targets, the improvement can be up to 15.2%. For wafers that did not meet, but moved closer toward the new targets, the improvement is around 8.2%.We estimate that the process modifications alone contributed about 8% yield improvement. Our results demonstrate that the Yield Optimizer is a powerful tool for improving product yield.

1 Introduction

In semiconductor field, high yield drives Fabs to constantly seeking better and more stable processes. Given the complexity and multiple steps the processes involve, it is difficult to model tool level activity and the whole productions line simultaneously. Here we introduce the NeuMath Yield Optimizer™, a powerful software tool that analyzes the relationships among in-process metrology readings and End-of-Line Yield and electrical test results for any semiconductor product family and recommends changes to the in-process metrology targets to optimize the average End-of-Line results for that product family. The Yield Optimizer uses advanced mathematical methods, proprietary algorithms and neural networks to analyze this data to develop a robust model that can be used to predict end-of-line results and to recommend metrology targets that will result in maximum yield or optimal end-of-line results [1]. As the source of its recommendations, it uses in-process metrology measurements, and End-of-Line yield, die sort and electrical test results that are usually readily available, though often underutilized in today's semiconductor manufacturing facilities,. The object the Yield Optimizer models is the whole production line, instead of single productions tools. Coupled with tool-level run-to-run controller, such as Dynamic Neural Controller [2], the Yield Optimizer will be able to affect the tool level response by setting optimal targets according to the current production conditions.

In this paper we describe significant yield improvement after installation of the Yield Optimizer at National Semiconductor Corp. First we describe the experimental setting and how process modifications are made according to Yield Optimizer recommendations. We then compare the yield before and after the modifications. A discussion section is then followed by conclusion remarks.

2 Methods

The Yield Optimizer was installed in mid-May 2005 on the CMOS product line. In this paper we used data from mid-May through mid-September 2005. Although the Yield Optimizer monitors 15 products in total, process modifications are made only on a particular product, Product 1, which is the main concentration of the test. In this paper, yield refers to percent-good-die (good-bins in Yield Optimizer screenshots).

Other process improvements, outside the scope of this study and independent of the Yield Optimizer, might have contributed somewhat to the yield improvement over the full four-month period. We assume that those improvements and modifications are implemented at random and are not dependent on this beta test. We realize that it is hard to distinguish the causes of final yield improvements; however, we reason that if a yield improvement shows a clear correlation with Yield Optimizer's recommendation and timeline of the modifications, it is reasonable to attribute the improvement to the Yield Optimizer. In this paper, we estimated the contribution of process modifications by the difference between the observed yield with and without the process modifications.

3 Process Modifications

During the four-month evaluation period, process modifications were implemented from July 6th to July18th (week 10 in Figure 1). Four independent modifications are made at different levels, namely contact level, metal 2 level and top via level. Because of the serial process nature, the first two modifications started to impact the top via level on July 15th and 18th respectively (as shown in Figure 1). In this section we list the details of how those modifications are decided upon based on Yield Optimizer recommendations.

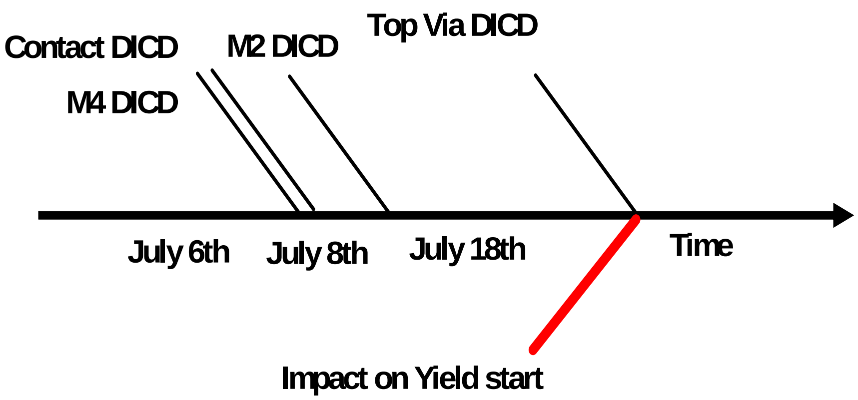


Fig. 1. Scheme of the timeline of the process modifications.

3.1 Contact DICD

The first lot to have the Contact DICD change implemented had its Contact DICD measured on July 8. Prior to this change, on July 5th, the top optimization from the Yield Optimizer recommended this change along with several other items, combining for approximately a 20% increase in yield (good-bins). Figure 2 shows a screenshot from Yield Optimizer. Figure 3 shows a drill down screen from the Figure 2's screen. It listed the contribution of each recommended action. The Contact DICD was predicted to be individually responsible for about 10% increase in yield. Figure 4, the sensitivity analysis of Contact DICD confirms this prediction. Based on those analyses, Contact-DICD modification was implemented.

3.2 Top Via CD

The first lot for which the change to Top Via DICD was implemented had its Top Via DICD measured on July 18. Top Via DI-DELTA is recommended on July 14th as a change along with M2 FICD, combining for a 4% increase in yield. This change was implemented by changing the DICD target from .37 to .36, since it is not possible to change the delta directly. The breakdown of the best optimization, shows that the Top Via was the only contributor to yield, providing all of the 4% increase in yield. M2 FICD improved some of the other outputs. The sensitivity results for the Top Via CD show the same trend for improvement in yield.

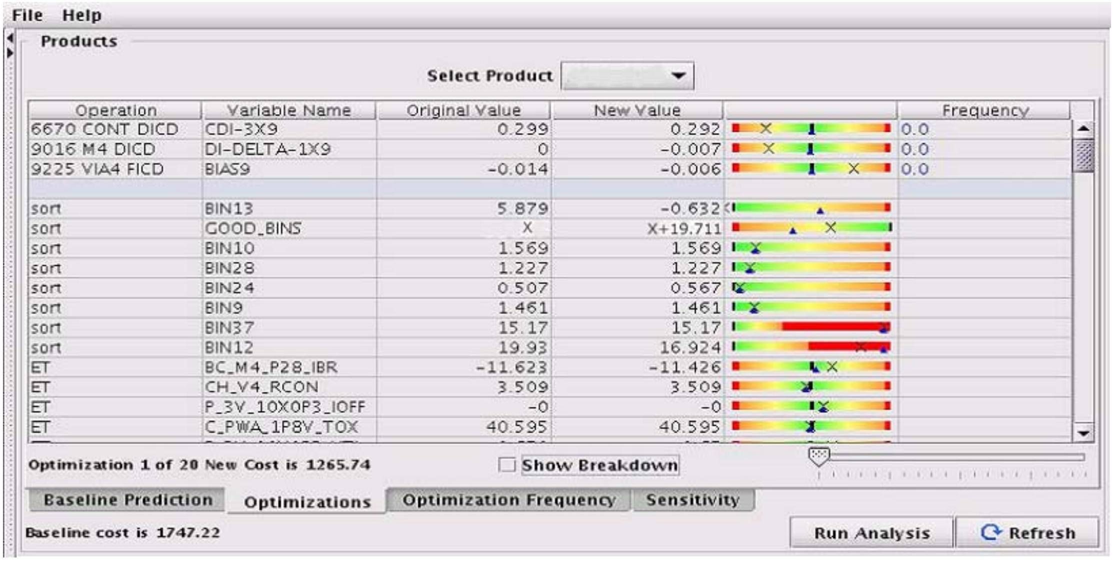


Fig. 2. Screen shot of the top optimization for Product 1 from Yield Optimizer on 07/05/2005. The rows before the shaded line are recommended operation modifications. Contact DICD is recommended for changed from original value 0.299 to new value 0.292. Rows below the shaded lines show how yield and electric test results will change upon the modifications (real number of original value for GOOD_BIN is replaced by X). The color bars on the right reflect the original value (the blue triangular) and new value (cross).

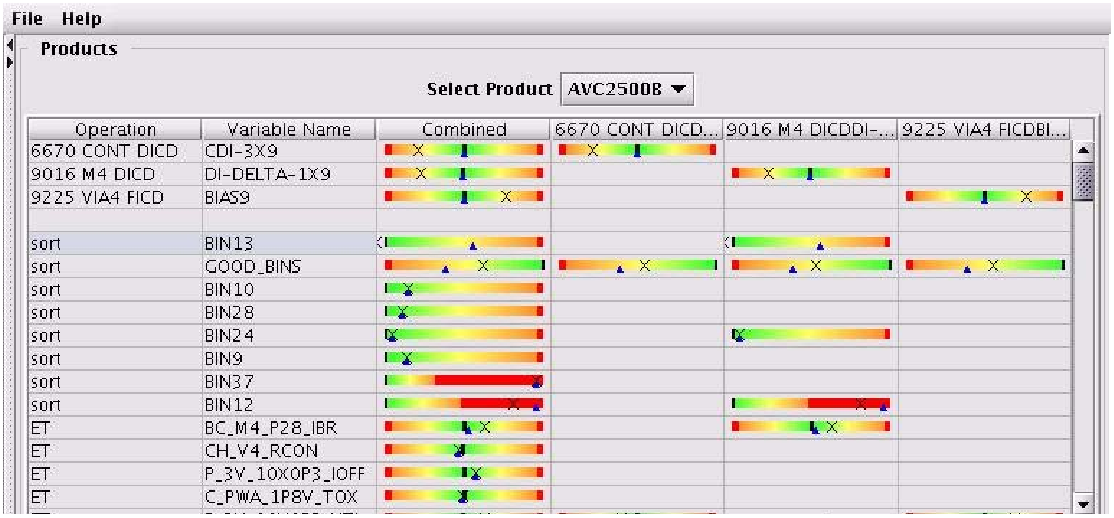


Fig. 3. Screenshot of a drilldown from Fig. 2, with details of individual contribution of each recommended action.

3.3 M2 DICD

The change to M2 DICD was implemented on July 6. Due to the limitation of the fab processes, DICD changes are typically implemented as corresponding FICD changes. On July 5, the Yield Optimizer predicted that there would be no change in yield for implementing this change. On June 28, the sensitivity analysis showed approximately a 1% improvement in yield if the FICD were changed from 0.279 to 0.272. This change, however, was not among any of the optimization results.

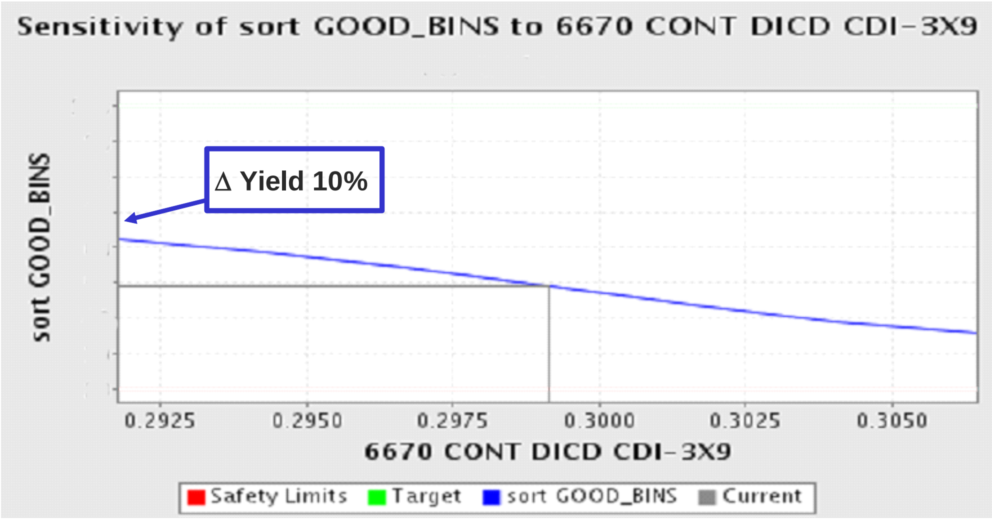


Fig. 4. Sensitivity screenshot of yield (good-bins) to contact DICD. Current value is indicated by gray project lines.

However, for Top Via adjustment, M2 FICD was recommended in the top optimization. Further analysis shows that M2 FICD will improve other output variables but not yield. This feature in Yield Optimizer gives user the flexibility to consider more than one output factors and weight them accordingly. For example, when a fab situation calls for speed instead of high yield, user can adjust the model by weight speed than yield more to get sensible recommendations.

Because of the Yield Optimizer does not predict M2 FICD has major impact on the final yield, we expect that this modification will not contribute to significant yield improvement.

3.4 M4 FICD

Similarly, the Yield Optimizer recommended a M4 DICD change from 0.28 to 0.289. A minor improvement of 0.1% of yield is expected from this adjustment.

3.5 Summary of process modifications

In short, from July 6th to July 18th, the following changes were made

1. Reduce top via DICD from 0.370 to 0.360
2. Reduce contact DICD from 0.299 to 0.292
3. Reduce M2 DICD from 0.244 to 0.237
4. Increase M4 FICD from .28 to 0.289

These modifications have been left in place and can be seen in the data, which we describe in the next section. On average, the new targets associated with these changes are being met in the later data, providing a reasonable data sample from which to draw conclusions.

4 Results

4.1 Compare Yield Before and After the Process Modifications

We find that the yield increases significantly after the process modification. Figure 10 shows the weekly average product yield for Product 1. The week of 5/5/2005 is counted as week 1, and data end on week 22 (9/25/2005). Overall, the yield shows an increase over time, while the trend after the modifications is more stable. The average yield level after the modifications is at a significant higher-level compare to before the modifications. Comparing Before-modifications to After-Modification, (after all three modifications started to impact the yield), the average yield is 8.2% (Table 1).

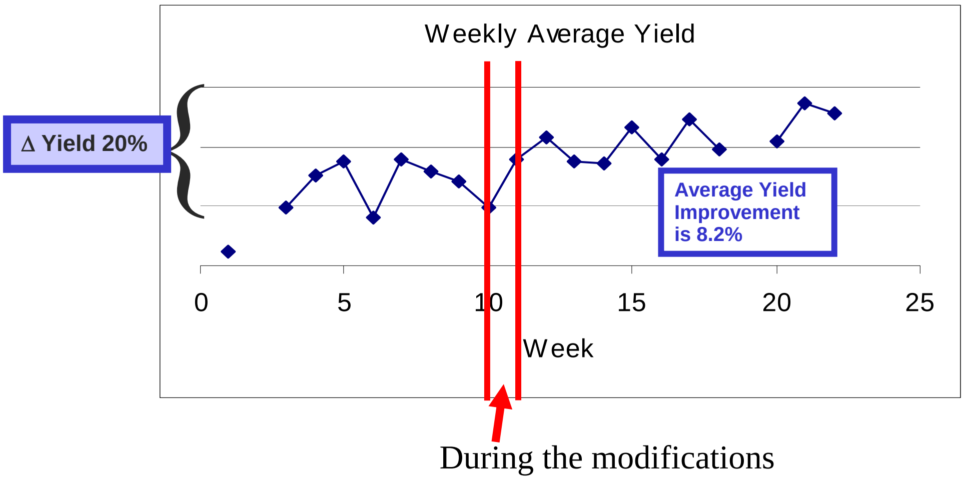


Fig. 5. Weekly average of yield from 5/5/05 to 9/25/2005. The modifications happened between week 10 and 11, indicated by the two red vertical lines. Each y grid line represents 20% yield increase

In Table 1, yield changes during and after the process modifications are listed. The data are grouped into 4 groups, namely “no changes”, “M2 DICD Only”, “Top Via DICD Only”, “TopVia and M2 DICD”, and “All three changes”. The “no changes” group includes all the wafers before any modification is implemented. The “All three changes” group includes all the wafers that are affected by the three modifications. Other groups refer to wafer that are affected by difference combination of the modifications during the modification implementations. Because of serial nature of semiconductor process and complex wafer routing, each process modification has individual time delay to impact the yield. Therefore those groups reflect the yield changes during the modification implementations. Table 1 also includes the average metrology reading for the three variables subject to changes.

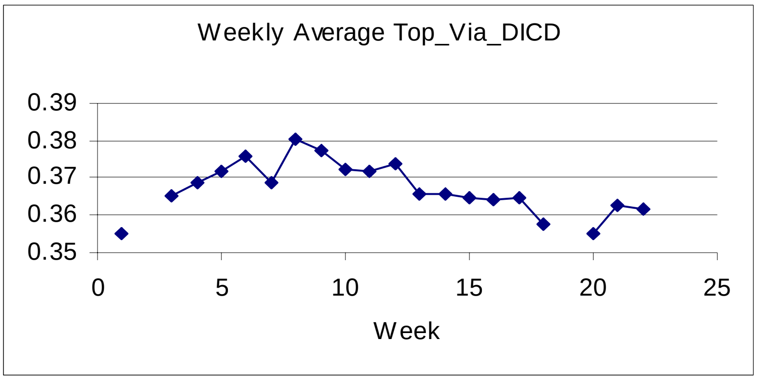
Table 1. Comparison of yield before, during and after the process modifications

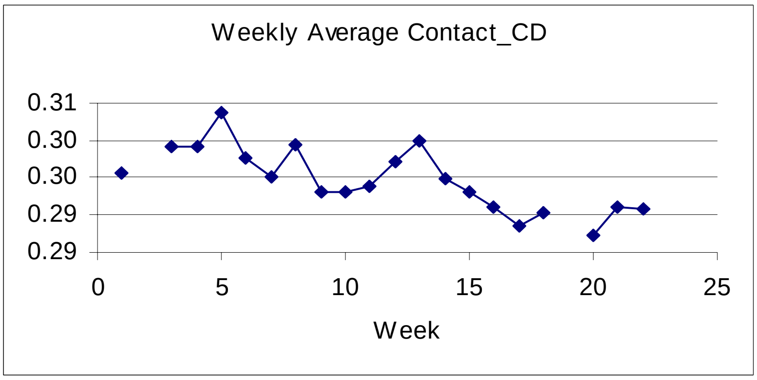
Group	Delta Yield	Top_Via_DICD	Contact_CD	M2_DICD	M4_FICD	Lots
No Changes	**0 = Baseline**	**0.371**	**0.297**	**0.250**	**0.276**	**30**
(stand error)		0.001	0.001	0.000	0.001	
Changed Only M4 FICD	**5.22**	**0.372**	**0.293**	**0.251**	**0.282**	**6**
(stand error)		0.002	0.001	0.001	0.002	
Changed M2 DICD and M4 FICD	**7.51**	**0.386**	**0.294**	**0.247**	**0.273**	**1**
(stand error)		0.000	0.000	0.000	0.000	
Changed Top Via and M4 FICD	**5.49**	**0.371**	**0.307**	**0.245**	**0.287**	**1**
(stand error)		0.000	0.000	0.000	0.000	
Changed Top Via, M2 DICD and M4 FICD	**8.73**	**0.366**	**0.296**	**0.241**	**0.280**	**9**
(stand error)		0.002	0.001	0.002	0.001	
All 4 Changes	**8.16**	**0.362**	**0.291**	**0.242**	**0.286**	**29**
(stand error)		0.001	0.000	0.001	0.001	

We noticed that in Table 1, the yield start to increase during the process modifications. In fact, all groups during the modification show a 4-5% yield increase. As we pointed out in the sensitivity analysis in later sections, changing those metrologies in the right direction should improve the yield even before the metrology reading reach the optimal setting. Our results confirm the sensitivity analysis from Yield Optimizer.

4.2 Compare the Yield for Lots Which Approached the Targets to Lots Which Did Not Meet the Targets

It is worth noting that the four metrologies reach their new target gradually. The time course of the metrology reading closely corresponds to the steady yield improvement (Figure 5, with three modifications showing). This close relationship indicates that the yield improvement is largely due to the metrology modification instead of other independent process modifications.





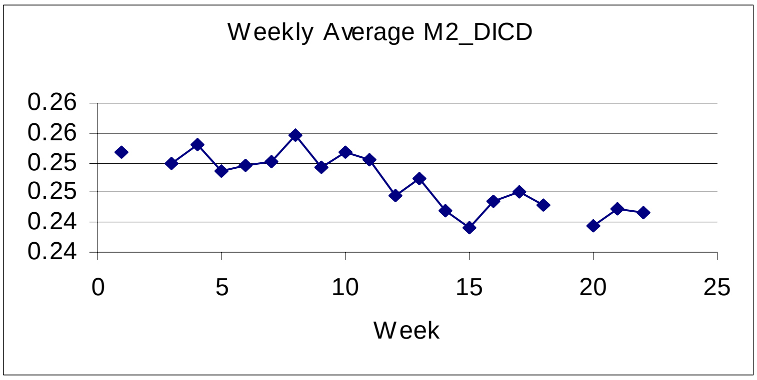


Fig. 6. Weekly average of metrology Top Via DICD, Contact CD and M2 DICD. Top Via DICD is modified to the lower value of 0.36. Contact CD is modified to the new target of 0.292. M2 DICD is modified to the new target of 0.237. All modifications happened between week 10 and 11.

Although Figure 5 shows that the metrologies do merge towards their new targets, upon close inspection, there are significant in-lot variations for those metrology readings. Based on the Yield Optimizer, those wafers with those metrologies hit the new targets should have higher yield than those missed the targets. To confirm this hypothesis, we divided the wafers *after* the modifications into groups according to which target it hits.

In performing this analysis, we used considerably tighter tolerances on the new targets to classify a target as being met or not met. For the Top Via CD, we considered new target of 0.36 met if the measured value fell between 0.356 and 0.364. For the Contact CD, we considered the new target of 0.292 met if the measured value fell between 0.291 and 0.293. For the M2 DICD, we considered the new target of 0.237 met if the measured value fell between 0.235 and 0.239. All measured values outside of these target ranges were considered as not meeting targeted values. Table 2 includes results from all wafers that were impacted by at least one modification.

GROUP	Δ Yield	TOP VIA_DICD	CONTACT_CD	M2_DICD	M4_FICD	LOTS
Change Recommended		(0.370 to 0.360)	(0.299 to .0292)	(0.244 to 0.237)	(0.280 to 0.289)	
Before Test: No Changes	0% (Baseline)	0.371	0.297	0.251	0.276	30
After test: Approach targets but none hit target	8.24%	0.370	0.293	0.243	0.283	11
Hit Only M4 FICD	8.54%	0.368	0.298	0.245	0.289	2
Hit Only M2 DICD	5.84%	0.380	0.299	0.235	0.281	1
Hit Only Contact	5.08%	0.366	0.292	0.245	0.282	8
Hit Only Top Via	9.29%	0.363	0.299	0.243	0.284	2
Hit Contact and M4 FICD	5.11%	0.367	0.292	0.249	0.286	3
Hit Contact and M2 DICD	8.12%	0.346	0.291	0.239	0.281	1
Hit Top Via and M4 FICD	12.64%	0.359	0.290	0.246	0.289	2
Hit Top Via and M2 DICD	12.11%	0.361	0.287	0.237	0.286	3
Hit Top Via and Contact	6.87%	0.361	0.292	0.244	0.282	7
Hit All but M2 DICD	9.94%	0.360	0.292	0.243	0.290	5
Hit All but Top Via	15.22%	0.367	0.292	0.236	0.296	1

Table 2. Yield comparison of wafers that hit the new targets and those misses the new targets. New target for Top Via DICD is 0.360, for contact CD is 0.292 and for 0.237

First of all, we noticed that all groups, including the “Approach targets but none hit targets”, show over 5% increase compare to baseline yield before any modifications (the baseline). We attribute the improvement to the quick converge of Contact CD to the new target, since this group already has an average Contact CD equal to 0.293. Further more, when the new Contact CD, the new M4 FICD and the new M2 DICD targets are reached individually**,** there is no appreciable further change in yield. These results may stem from very different reasons. For Contact CD, the “hit only contact DICD” group only improved to 0.292 from 0.293. From the sensitivity curve (Figure 4), no significant further yield improvement is expected from such a minor metrology change. For M2 DICD, based on Yield Optimizer, we do not expect it to be a major contributor to the yield improvement. When any two of the three targets are met, there is a 5.11% to 12.64% improvement in yield. When three out of four targets are met, the improvement is up to 15.22%. There are no lots in the dataset for which all four of these new targets are reached with the desired accuracy.

To further illustrate our observation of the relationship between approaching the targets and the final yield, we plot the yield vs. the Euclidean distance from the targets (Figure 6). There is a clear trend that when the distance from the targets decrease, the yield increases.

4.3 Estimate impact of other factors:

The only other known factors which may impact the final yield during the study are improvements on process metrology percent clean dies. Efforts were spent on improving 25 different percent clean dies throughout the production line. During the investigation of the impact of these efforts on the final yield, we found no clear correlation between 25 percent_clean_die inputs and yield are found during the study period. One example is shown on the right. None significant contribution from percent_clean_die on yield improvement reported here (Figure 7).

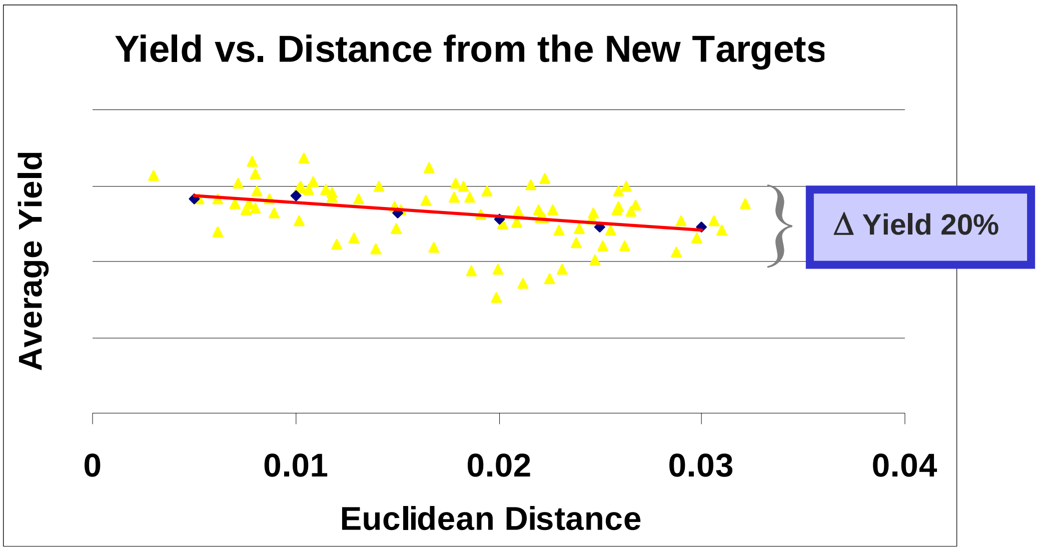


Fig. 7. Yield vs. Distance from the new targets. The y grid line stands for 20% yield delta. Each dot reflects a lot measured. The red line is the regression trend line.

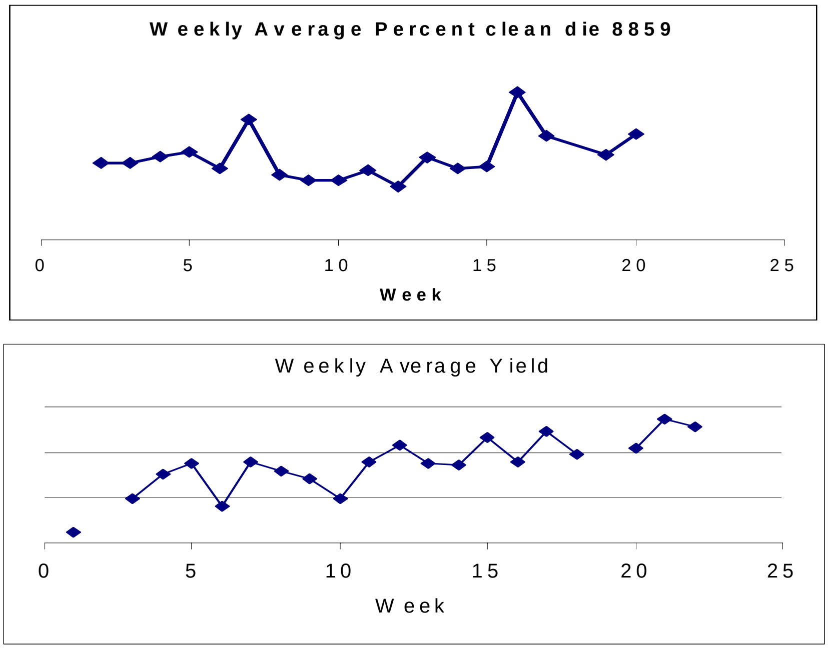


Fig. 8. Example of weekly Percent clean die compared with weekly average yield.

Out of all percent clean dies, only one (1488) showed impact on yield, which increased from 61.73 to 95.610 at around 7/21. We estimated that the 1488 percent clean die contributed to about 2.907% yield improvement, where the Yield Optimizer recommended process modifications contributed 10.9%, i.e, additional 8 %. This estimation is calculated from Table 3.

Table 3. Impact of percent clean die improvement on End of Line Yield.

	Target Values		
Variable	**Baseline**	**Scenario 1**	**Scenario 3**
Top Via DICD	0.370	0.370	0.360
Contact DICD	0.299	0.299	0.292
M2 DICD	0.244	0.244	0.237
M4 FICD	0.280	0.280	0.289
1488 Pct Clean Die	61.730	95.610	95.610
Yield Change	Baseline	2.907	10.921

Table 3 illustrates 2 scenarios. The baseline shows the metrology and yield readings before any process modifications. In Scenario 1, yield improvement of 2.907 over the baseline reflects the condition that Percent clean die improved from 61.730 to 95.610, but all metrologies remains the same. In scenario 3, the percent clean die remains the same, but the metrologies approached their new targets, the total yield improvement over the baseline is 10.921. The additional yield increase is due to the process modification.

5 Discussion

Our results demonstrated significant improvement in product yield after the process modification based on the Yield Optimizer recommendation. For wafers that met most of the new targets, the improvement can be up to 11.1%, for wafers that did not met but got closer toward the new targets, the improvement is around 5.95%. Overall, we saw improvements in lot Yield of up to 15.2% after modifications vs. before modifications. The results indicated the importance of a fast convergence onto the new metrology targets. We highly recommend deployment of a process run-to-run controller, such as the NeuMath Dynamic Neural Controller™ in conjunction with the Yield Optimizer to achieve fast and stable process improvement.

This study was carried out in production line, where a control of experiments was not possible, or cost effective. We realize that other independent improvements were made outside of this beta test's scope, which were incorporated post facto into the analysis and accounted for 2.9% Yield increase. Special attention was paid to separate the impacts from other factors. We only claimed the contribution of Yield Optimizer when there was a clear correlation between the recommended process modifications and the yield improvement.

6 Conclusion

Overall, the Yield Optimizer made four suggestions for improvement that were implemented on a somewhat consistent basis in production. On average 8.2% yield increase is shown after the process modifications. We estimate that consistent Percent clean die improvement contributed to about 2.9% of yield improvement; consistent process modifications contributed additional 8%. Best result (15.2%) yield increase is observed when most of the new targets are met.

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